Optimal VLSI Architectural Synthesis: Area, Performance and Testability (The Springer International Series in Engineering and Computer Science)

Catherine H. Gebotys, Mohamed I. Elmasry

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Optimal VLSI Architectural Synthesis: Area, Performance and Testability (The Springer International Series in Engineering and Computer Science) Catherine H. Gebotys, Mohamed I. Elmasry Although research in architectural synthesis has been conducted for over ten years it has had very little impact on industry. This in our view is due to the inability of current architectural synthesizers to provide area-delay competitive (or "optimal") architectures, that will support interfaces to analog, asynchronous, and other complex processes. They also fail to incorporate testability. The OASIC (optimal architectural synthesis with interface constraints) architectural synthesizer and the CATREE (computer aided trees) synthesizer demonstrate how these problems can be solved. Traditionally architectural synthesis is viewed as NP hard and there fore most research has involved heuristics. OASIC demonstrates by using an IP approach (using polyhedral analysis), that most input algo rithms can be synthesized very fast into globally optimal architectures. Since a mathematical model is used, complex interface constraints can easily be incorporated and solved. Research in test incorporation has in general been separate from syn thesis research. This is due to the fact that traditional test research has been at the gate or lower level of design representation. Nevertheless as technologies scale down, and complexity of design scales up, the push for reducing testing times is increased. On way to deal with this is to incorporate test strategies early in the design process. The second half of this text examines an approach for integrating architectural synthesis with test incorporation. Research showed that test must be considered during synthesis to provide good architectural solutions which minimize Xlll area delay cost functions.

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